IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Mailloux, et al.

Serial No.: 08/984,563

Filed: December 3, 1997

For: BURST/PIPELINED EDO MEMORY DEVICE

§ Group Art Unit: 2751
§ Examiner: Kim, H.
§ Atty. Docket: 95-0653.03

INFORMATION DISCLOSURE STATEMENT

Certificate of Mailing (37 C.F.R.§ 1.8)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on the date below:

12/29/98 Peggy Boyd-Fuster
Date Signature

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In compliance with the duty of disclosure under 37 C.F.R. § 1.56, Applicant[s] respectfully request[s] that this Information Disclosure Statement be entered and that the references listed on the attached Form PTO-1449 be considered by the Examiner and made of record. As the references are cumulative from the parent case, copies of the listed references are not enclosed.

In accordance with 37 C.F.R. § 1.97(b), this Information Disclosure Statement is not to be construed as a representation that a search has been made or that no other possible material information as defined in 37 C.F.R. § 1.56(a) exists.

The following references are submitted for the Examiner's review:

U.S. Patents

U.S. Patent No.	Issue Date	Inventor
5,357,469	10/18/94	Sommer et al.
5,268,865	12/7/93	Takasugi
4,618,947	10/21/86	Tran et al.
5,267,200	11/30/93	Tobita
4,344,156	8/10/82	Eaton et al.

47-48, (September 1994)

Dave Bursky, "Novel I/O Options and Innovative Architectures Let DRAMs Achieve SRAM

Performance; Fast DRAMS can be swapped for SRAM Caches", Electronic Design, Vol. 41, No. 15,
Cleveland, Ohio, pp. 55-67, (July 22, 1993)

Shiva P. Gowni, et al., "A 9NS, 32K X 9, BICMOS TTL Synchronous Cache RAM With Burst Mode

Access", IEEE, Cutsom Integrated Circuits Conference, pp. 781-786, (March 3, 1992)
S3 Incorporated, "S3 Burst Mode DRAM", 6/93, 2 pages

Electronic News "Mitsubishi Samples 16M Synch DRAM", 10/25/93, pgs. 3-4

""DRAM 1 Meg X 4 DRAM 5BEDO Page Mode",", 1995 DRAM Data Book, pp.1-1 thru 1-30,,
(Micron Technology, I)

NEC "Command Truth Table" March 15, 1993

Samsung Electronics "KM48SV2000 Preliminary CMOS SDRAM" Rev.1(Mar, 1993), pgs. 7-8

This Information disclosure Statement is being submitted after the mailing of the first Office Action, but before the mailing of a Final Rejection or Notice of Allowance. The Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) of $240.00 and any additional fees which may be required to Micron Technology, Inc. Deposit Account No. 13-3092, Order No. 95-0653.03.

If there are any matters which may be resolved or clarified through telephone interview, the Examiner is respectfully requested to contact Applicant's undersigned attorney at the number indicated.

* * * *

A Form PTO-1449 is enclosed herewith.

Respectfully submitted,

Date: 12-29-98

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